

CLAIMS

What is claimed is:

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2 *as* 1. A method for increasing yield of usable memory locations in an embedded memory
3 device, the method comprising:

4 providing a cache for a memory unit;

5 determining when an access is made to a failed bit memory location in the memory unit;

6 and

7 substituting a memory location in the cache for the failed bit memory location when the
failed memory bit location is accessed.

1 2. The method of claim 1 wherein determining when an access is made further comprises
2 identifying each failed bit location in the memory unit and storing each failed bit location in the
3 cache.

1 3. The method of claim 2 wherein storing further comprises storing each failed bit
2 location in a look-up table.

1 *Sub*
2 *as* 4. The method of claim 3 wherein determining further comprises comparing a memory
location being accessed to identified failed bit locations.

1 5. The method of claim 2 wherein identifying each failed bit location further comprises
2 performing a pre-scan operation on the memory unit.

1 13. The method of claim 8 wherein the memory unit further comprises a DRAM unit.

1 14. The method of claim 8 wherein the cache further comprises an SRAM unit.

1 15. An embedded memory device with increased yield of usable memory locations, the
2 embedded memory device comprising:
3 a memory unit;
4 a cache coupled to the memory unit, and
5 a memory control unit coupled to the memory unit and the cache, the memory control unit
6 determining when an access is made to a failed bit memory location in the memory unit, and
7 substituting a memory location in the cache for the failed bit memory location when the failed
8 memory bit location is accessed.

1 16. The embedded memory device of claim 15 wherein the memory unit further
2 comprises a DRAM.

1 17. The embedded memory device of claim 15 wherein the cache further comprises an
2 SRAM.

1 18. The embedded memory device of claim 15 wherein the memory control unit further
2 identifies each failed bit location in the memory unit and stores each failed bit location in the
3 cache.

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1 6. The method of claim 1 wherein providing a cache further comprises providing an
2 SRAM.

1 7. The method of claim 1 wherein the memory unit further comprises a DRAM unit.

1 8. A method for increasing yield of usable memory locations in an embedded memory
2 device, the method comprising:

3 performing a memory pre-scan operation on an embedded memory device to identify each
4 failed bit location in the embedded memory device; and
5 swapping a memory location within a cache for a failed bit location.

1 9. The method of claim 8 further comprising providing the cache between a memory unit
2 and a memory control unit in the embedded memory device.

1 10. The method of claim 8 further comprising storing each failed bit location in a look-
2 up table in the cache.

1 11. The method of claim 8 wherein swapping a memory location further comprises
2 swapping when an access attempt is made to a failed bit location.

1 12. The method of claim 11 further comprising swapping by a memory control unit for
2 the embedded memory device.

